REMARKS

In response to the above-identified Office Action, Applicants seeks reconsideration of the rejections. In this response, no claims have been added, no claims have been cancelled, and no claims have been amended. Accordingly, Claims 1-10 are pending.

Claims Rejected Under 35 U.S.C. §102

The Examiner has rejected Claim 1 and Claim 3 under 35 U.S.C. §102 as anticipated by Deschaine, U.S. Patent No. 5,901,024 ("Deschaine"). Applicants respectfully traverse this rejection.

The Examiner asserts that Deschaine discloses fixing a logical identifier for a signal line at an egress interface. Applicants have reviewed the cited passage of Deschaine, but is unable to discern a teaching or suggestion of fixing a logical identifier for a signal line at an egress interface. The cited passage deals merely with rerouting traffic to a spare line card when another line card fails, and the swapping of time slots in the logical mapping on the time slot and interchanger link. Applicants submit that placing the spare line card in a time slot previously occupied by the failing line card does not teach fixing a logical identifier for a signal line in an egress interface as claimed. Applicants note that Deschaine appears to teach a centralized switch fabric. Conversely, the claimed invention is applicable to a distributed switch fabric as that is the only environment where protection dependency exists. Because the entire line card is swapped out (rather than remapping of a signal line on the line card), the need for the claimed fixing does not exist in Deschaine. Withdrawal of the rejection of Claim 1 is respectfully requested. With respect to Claim 3, Claim 3 depends from Claim 1 and is at least patentable as depended on a patentable independent claim.

Claims Rejected Under 35 U.S.C. §103

The Examiner has rejected Claims 5, 6, 8 and 9 under 35 U.S.C. §103 as being unpatentable over Deschaine in view of Fan, U.S. Patent No. 6,643,269 ("Fan"). Applicants respectfully traverse this rejection.

With respect to Claim 6, Applicants respectfully submit that at a minimum the combination of Deschaine and Fan fails to teach or suggest "an egress time slot interchange (ETSI) module having a plurality of inputs, each input assigned a logical identifier which remains fixed after initialization." The Examiner has not pointed to and Applicants have been unable to identify any teaching or suggestion of this element in either of the cited references. The Examiner dismisses the element of the ETSI, but merely pointing to Figure 2 of Deschaine and specifically the text "to time slot interchangers." This text fails to teach or suggest the element claimed. Setting aside the issue of whether this text would be sufficient to teach an ETSI module at all, it clearly fails to teach or suggest the fixation of the logical identifier after initialization as claimed. For at least this reason, Claim 6 is patentable over the references of record.

Claims 8 and 9 are at least patentable as dependent on patentable independent claims. Referring finally to Claim 5, Applicants respectfully submits that the addition of Fan fails to cure the deficiency discussed above in connection with Deschaine. Accordingly, Claim 5 is patentable as dependent on patentable independent claim.

In view of the foregoing, it is respectfully requested that the rejection under 35 U.S.C. §103 be withdrawn.

Respectfully submitted,

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Dated: August 10, 2004 By: Thomas Coester

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on August 10, 2004.

Susan M. Barrette 8/10/2004

Susan M. Barrette Date